



Connecting the World

DP 2.1 Certification & Test Solutions

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graniteriverlabs.com

Agenda

- DisplayPort Overview
- Receiver Test Methodology and Certification
- GRL Test Solutions



DisplayPort Overview

GRL



DisplayPort Specifications Comparison

Version	DP 1.4	DP 2.1
Supported Data Rates	8.1 Gbps (HBR3) 5.4 Gbps (HBR2) 2.7 Gbps (HBR) 1.62 Gbps (RBR)	20 Gbps (UHBR20) 13.5 Gbps (UHBR13.5) 10 Gbps (UHBR10) Backward compatible with DP 1.4 data rate
Coding	8b/10b	128b/132b, 8b/10b (for DP 1.4)
Cable loss	11dB@4.05GHz	Defined for different data rates
Reference Tx EQ	Pre-emphasis Level 0, 1, 2, 3 Swing Level 0, 1, 2, 3	3-tap FFE (P0~P15)
Reference Rx EQ	Optimized CTLE	Optimized CTLE + 1-tab DFE
Eye Height+Total Jitter (TP3_EQ) or Eye Mask(TP3_EQ)	Eye Height: 65mV Total Jitter: 500mUI	Eye Mask (TP3_EQ) UHBR10 – EH: 92mV / EW: 513mUI UHBR13.5 – EH: 112mV / EW: 540mUI UHBR20 – EH: 96mV / EW: 520mUI
Test Pattern	TPS4	PRBS31/PRBS15
Max Resolution Support	5K (5120x2800 @ 60Hz) - No DSC 8K (7680x4320 @ 60Hz) - With DSC	10K (10240x4320 @ 60Hz) - No DSC 16K (15360x4320 @ 60Hz) - With DSC

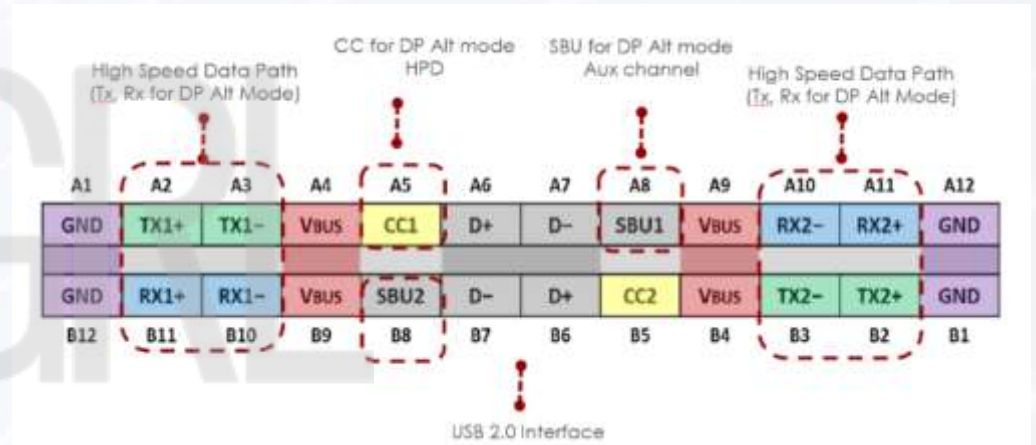
DP 2.1 Connector Types and DP Alt. Mode

■ DP 2.1 supports

- Enh Std DP Connector (Type1) supports up to 10Gbps (UHBR10)
- Enh Std DP Connector (Type2) supports up to 20Gbps (UHBR20)
- Enh mDP and Type-C connector support up to 20Gbps (UHBR20)

■ Pin assignments

- Pin C when using USB-C to USB-C (4 Lane)
- Pin D when using USB-C to USB-C or protocol converter (2+2)
- Pin E when using USB-C to DP (4 Lane)



By Granite River Labs

Receiver Test Methodology & Certification

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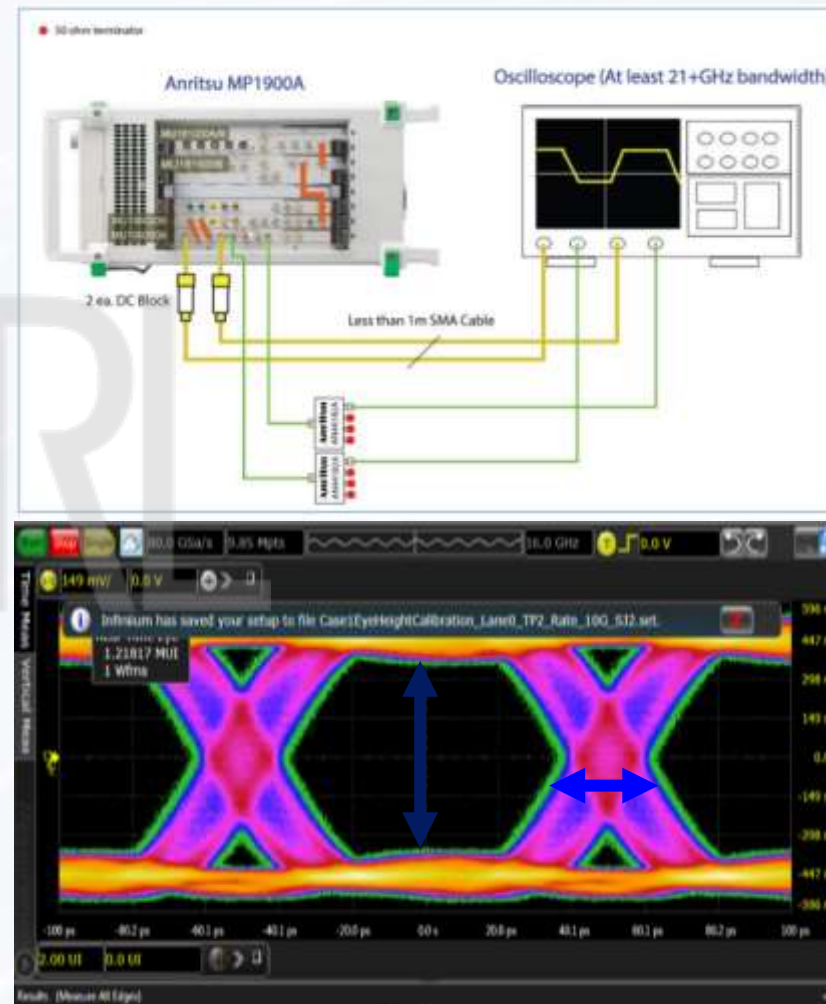
USB4 vs DP 2.1 vs DP 1.4 Jitter Parameter

Parameter	Topology	USB4	DP 2.1	DP 1.4
AC CM	TP1	100 mVpp @ 400MHz	100 mVpp @ 400MHz	100 mVpp @ 400MHz
Rj	TP1	Defined	Defined	Defined
Sj sweep	TP1	1, 2, 10, 50, 100MHz	1, 2, 10, 50, 100MHz	0.5, 1, 2, 10, 20, 100MHz
Sj fixed	TP1	n/a	n/a	Defined
DDj	TP1	Sweep TX FFE presets	Default preset 0	n/a
Eye height	TP1	Adjust VDIFF@ all Sj sweep Frequencies	Adjust VDIFF@100 MHz	n/a
Crosstalk	TP3	Defined	Defined	Defined
Tj	TP1 for U4/DP2 TP3 for DP1.4	Adjustment: - PJ for 100 MHz - RJ for all other Frequencies	Adjustment: - PJ for 100 MHz - RJ for all other Frequencies	Adjustment: SJFIXED Defined
ISI	IL @ fNyquist	Physical trace+Cable	Physical trace+Cable	Adjustable ISI Box
Eye diagram	TP3	Adjustment for EH: VDIFF Adjustment for EW: - SJ for 100 MHz - RJ for all other Frequencies	Adjustment for EH: VDIFF Adjustment for EW: - SJ for 100 MHz - RJ for all other Frequencies	Adjustment for EH: VDIFF

DP 2.1 Receiver JTOL Calibration Setup @ TP1

■ Pattern Generator Jitter Target Calibrated @ TP1

1. **DDj:** Use Preset0 for all calibration
2. **Rj:** Calibrate to the target value
3. **Sj:** Calibrate to the target value on 1/2/10/50/100MHz
4. **Total Jitter**
 - Apply for all targeted jitter
 - Required calibrate on each Sj frequency
 - Adjust Rj when Sj@ 1 ~ 50 MHz
 - Adjust Sj when Sj@ 100 MHz
5. **Eye Height**
 - Apply for all targeted jitter
 - Required calibrate on Sj@100MHz
 - Adjust VDIFF



Source: GRL Solution (GRL-DP21-SINK-AN)

Insertion Loss @ Nyquist

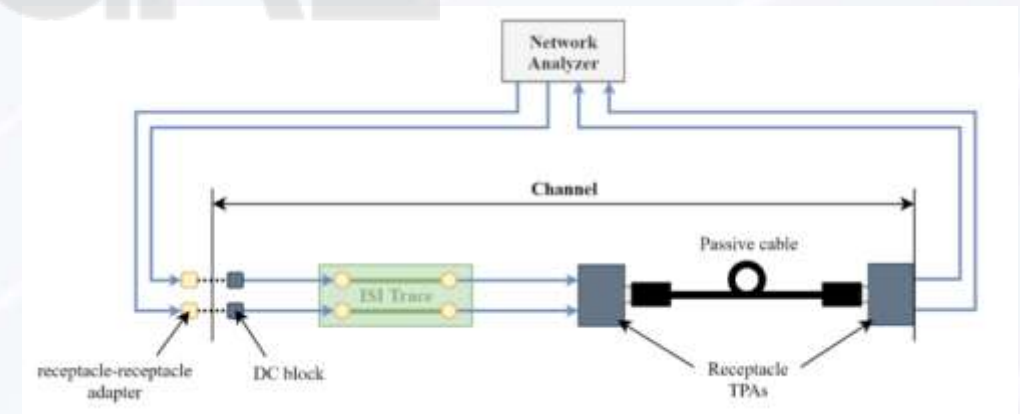
6. VNA Insertion Loss Target Calibrated

- Real Standard DP/ Type-C cable used
- Physical ISI trace
 - DC Block + ISI board + Test fixture



Cal Item	UHBR10	UHBR13.5	UHBR20
Nyquist Freq.	10GHz	6.75GHz	10GHz
IL@Nyquist	19dB	16.5dB	16.5dB

Note: all with +/- 0.5dB tolerance

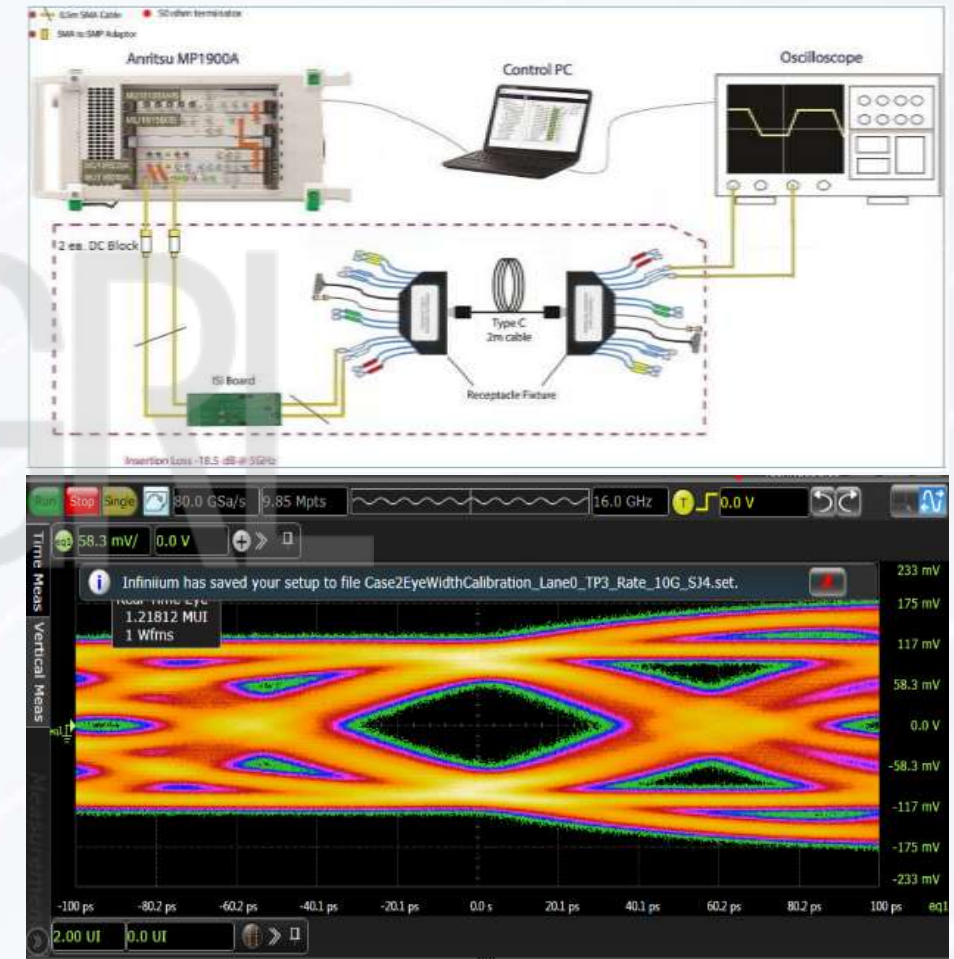


Source: DP2.1 Receiver PHY CTS

DP 2.1 Receiver JTOL Calibration Setup @ TP3

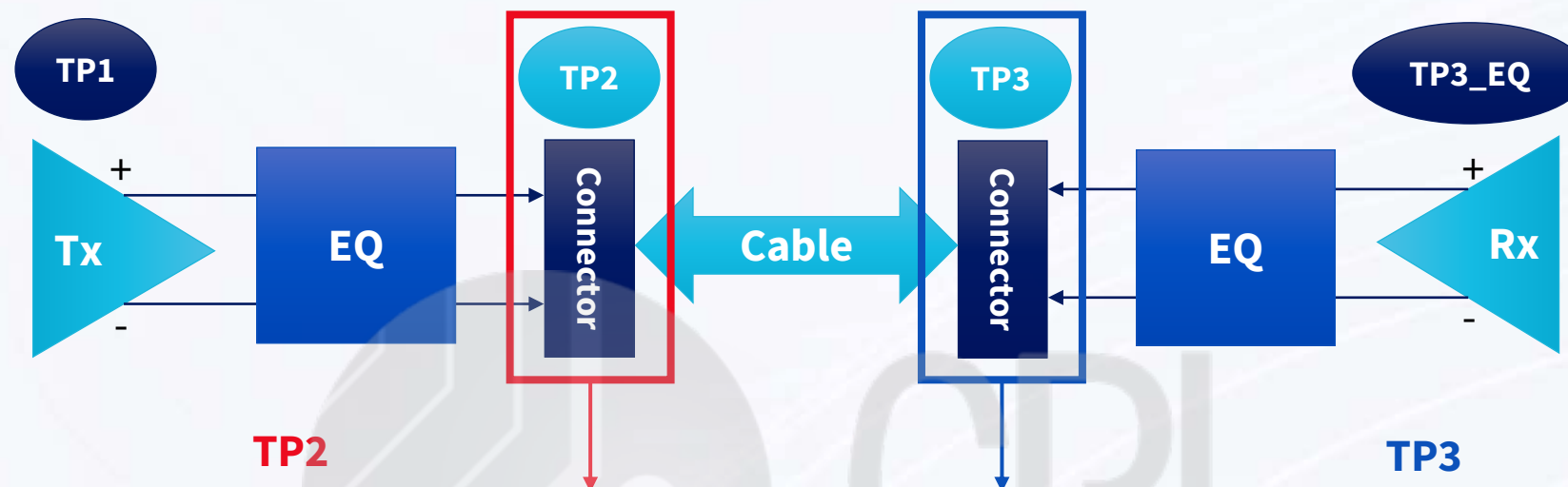
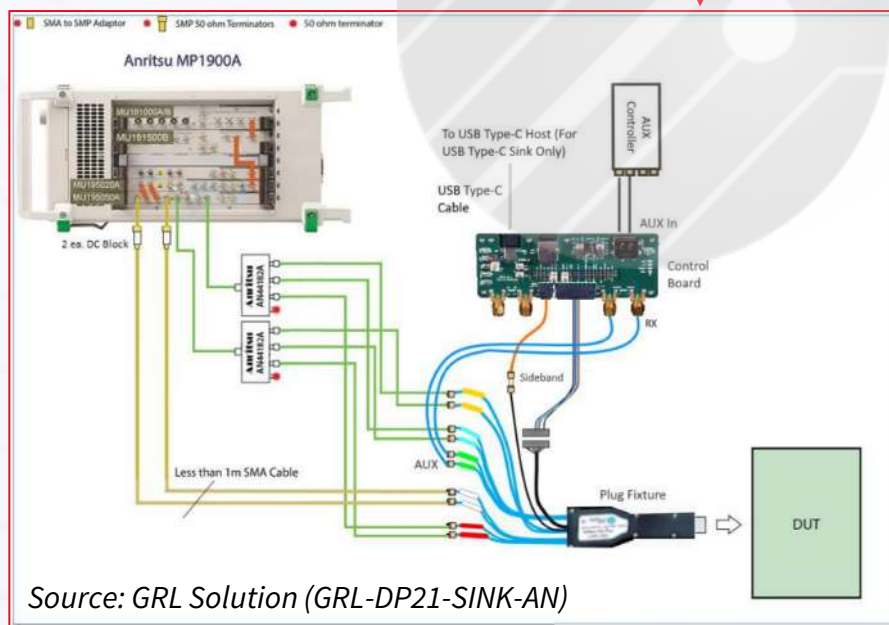
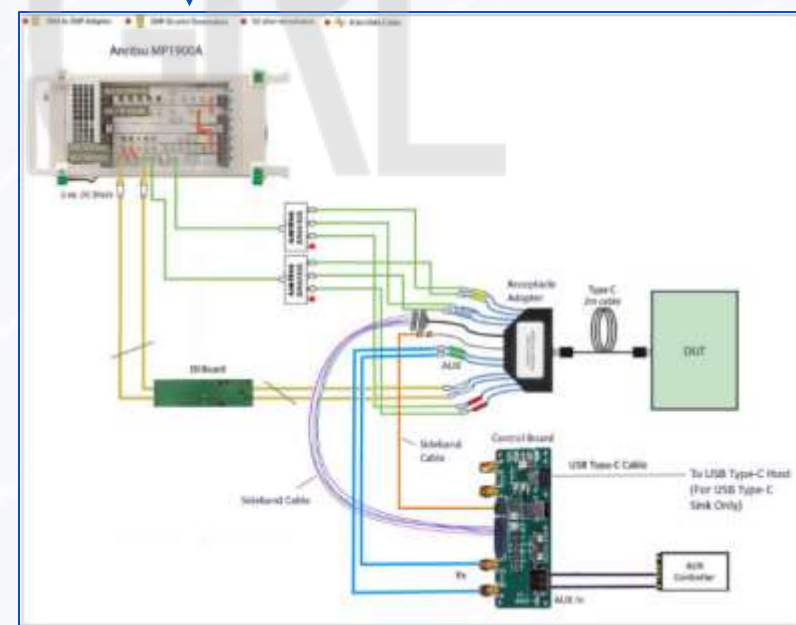
7. Eye diagram

- Apply for all targeted jitter
- Sweep 10 CTLE DC gains + DFE with FFE preset 0. And then select the one with highest $[EH * EW]$
 - Eye Height
 - Adjust VDIFF
 - Eye Width
 - Adjust R_j when $S_j@ 1 \sim 50$ MHz
 - Adjust S_j when $S_j@ 100$ MHz

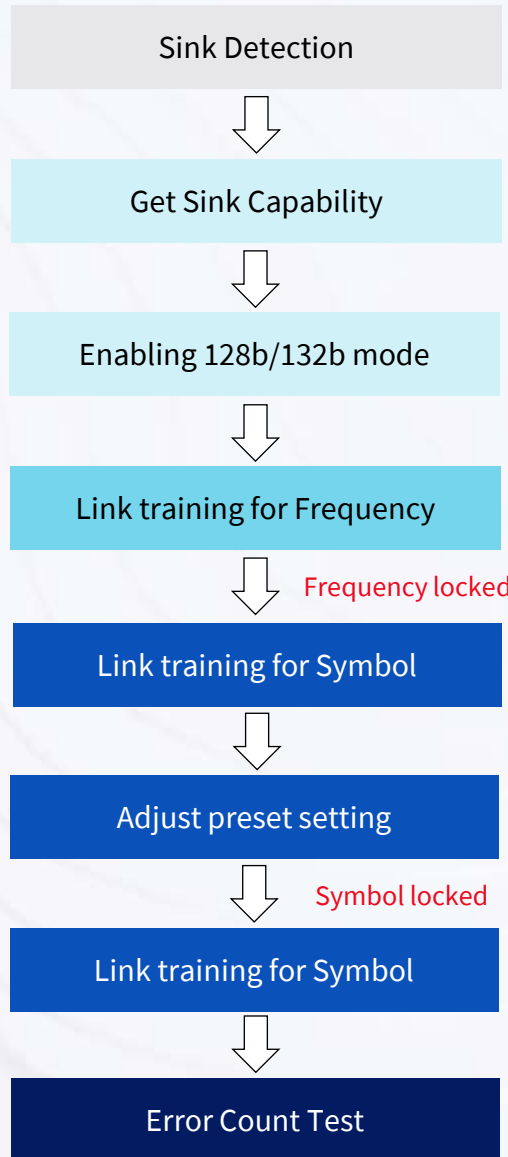


Source: GRL Solution (GRL-DP21-SINK-AN)

DP 2.1 Receiver JTOL Test Setup



DPCD Sequence for Rx PHY Testing



UHBR calibration data is applying BERT output signal.

1. Check UHBR capability.
2. Establish link at UHBR 128b/132b mode.

Set the BERT to D10.2 Pattern

1. Frequency lock

Set the BERT to 128b/132b_TPS2 Pattern

1. Symbol lock
2. Adjust the drive setting as requested by a Sink

Set the BERT to PRBS31 Pattern

1. Error count Test
2. Check each Sj frequency 1/2/10/50/100MHz

DP 2.0 Early Certification and UHBR Cable Certification

■ Source and Sink DUT (Early Certification)

- DP2.0 PHY Test
- DP2.0 Link Layer Test
- DP2.0 Interoperability Test
- DP1.4 Compliance Test

■ UHBR Cable Types

- DP40 (support up to UHBR10)
- DP80 (support up to UHBR20)

■ Cable Certification Test Items

- Insertion Loss Fit at Nyquist Frequencies (ILfitatNq)
- Integrated Return Loss (IRL)
- Integrated Total Crosstalk (IXT_DP)
- Differential to Common Mode Conversion
- Integrated Multi-reflection (IMR) - Informative
- Integrated Crosstalk on DP Lanes (IFEXT) – Informative
- Intra-Pair Skew
- Inter-Pair Skew – Informative
- Impedance
- CableID Test

What GRL can offer for DisplayPort?



DisplayPort 1.2/1.4
DisplayHDR 1.1,
Adaptive-Sync Certification



Assist customer on the **waiver**
document



DisplayPort 2.0
Test requirement or CTS
discussion. Early-stage
verification on PHY,
protocol...

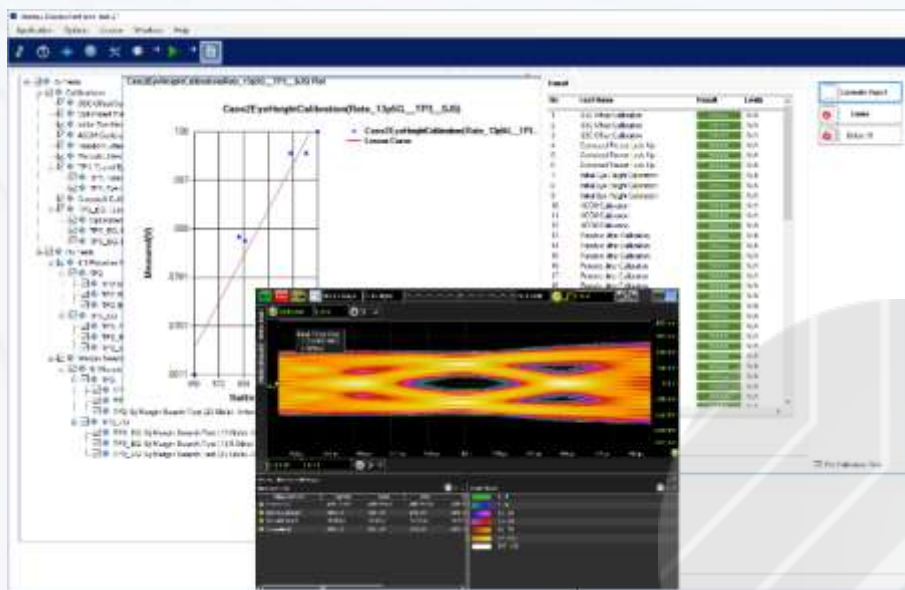


VESA Certified
GRL test solution
& Software development



GRL Test Solutions





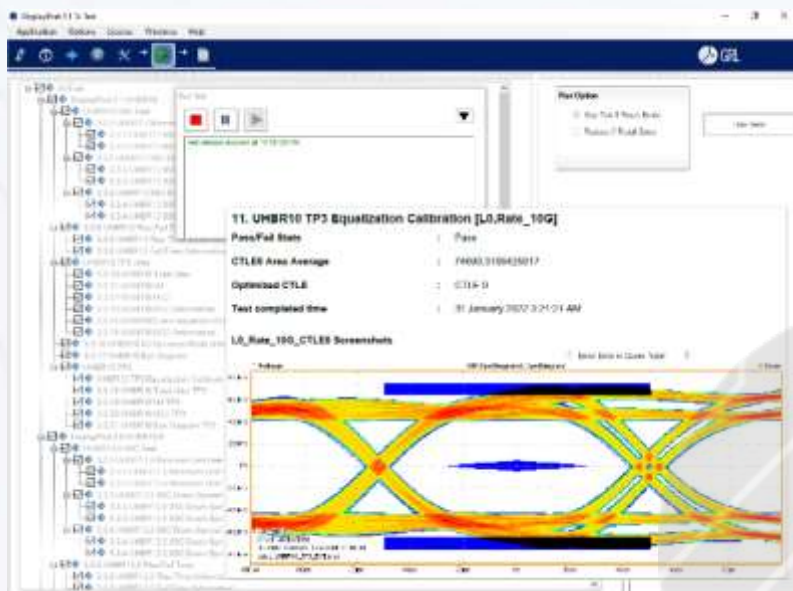
DisplayPort Receiver Calibration and Test Automation

An automated and efficient way to test your DisplayPort 2.0 Sink Device (GRL-DP21-SINK-AN, GRL-DP14-SINK-AN)

Overview

- Provides full compliance automation to test Sink products to the DisplayPort 2.0 and 1.4 standards
- Automatically calibrates BERT and Scope to create stressed eye for Sink Jitter Tolerance testing
- Compatible with Tektronix and other brands oscilloscopes paired with the Anritsu MP1900A BERT
- Fully integrated with high-speed test fixtures and AUX controller available from Wilder Technologies (sold separately)





Overview

- Provides full compliance automation to the DisplayPort 2.0 standard.
- Compatible with Tektronix and Keysight oscilloscopes.
- Flexible selection on test items and data rates (UHBR10, UHBR13.5, and UHBR20).
- DP 2.1 draft according to current CTS.
- Developing AUX automation.

DisplayPort 2.0 Transmitter Test Automation Solution

A quick and straightforward way to test and debug your DisplayPort 2.0 transmitter products efficiently (GRL-DP21-TX)

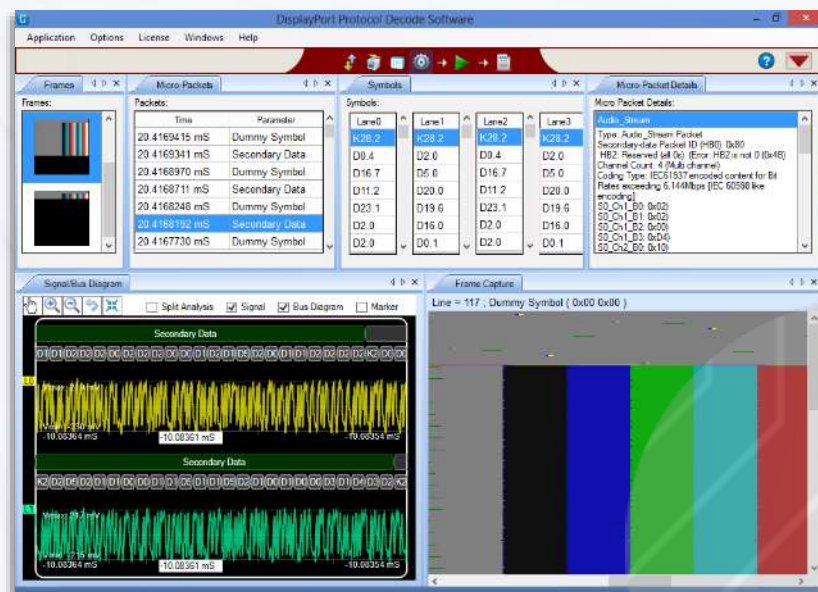


USB Type-C® Power Delivery Tester & Analyzer - EPR

One instrument for all your needs for validating compliance, inter-operability, and reliability of your designs

Overview

- Fully Integrated and Automated Compliance Testing Solution for the latest Power Delivery 3.1 Specification
- Backwards compatible with Power Delivery 3.0 and 2.0 Specifications
- Two independent ports (Source/Sink up to 240W each) for testing multiport devices
- All-in-one tester, integrated protocol exerciser, analyzer, e-load, power supply, Oscilloscope, and multimeters makes it less complex test setup
- Designed for reliability, robustness testing and beyond compliance testing
- Extensive API support to write custom test programs (C# and Python) to meet your unique testing requirements



Overview

- Provides detailed insight into main link & AUX transactions, including raw MST
- Seamlessly links physical layer signals to display port micro packets to display port stream to video frame

GRL-DP-DEC
GRL-DPAUX-DEC

Superior automation software for debugging DP related issues

Close to Technology, Close to You

- Silicon Valley HQ, 7 labs around the world, > 300 employees
- Recognized World Leader in Test Services and Automation Solutions for Connectivity and Charging



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Austin, TX

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Taipei

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Thank You!



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